Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A method for generating a command file of a group of design rule check (DRC) rules for being used by a layout verification tool to verify the design of an integrated circuit, the method comprising:

(a) selecting a process from a group of processes;

(b) setting a set of parameters; and

(c) extracting program codes from a plurality of modules according to the selected process and the set of parameters so as to generate a corresponding command file of DRC rules.

[c2] 2. The method of claim 1 further comprising:

(d) generating the plurality of modules, the plurality of modules comprising:

a header module comprising program codes for settings of a verification tool of different processes;

a variable module comprising program codes for setting fabrication parameters of different processes;

a layer module comprising program codes for setting layer definitions of different processes; and

an operation module comprising program codes of oper-

ation definitions of different processes.

[c3] 3. The method of claim 1 wherein the parameters comprise number of metal layers.

[c4] 4. The method of claim 1 wherein the parameters comprise number of poly-silicon layers.

[c5] 5. The method of claim 1 wherein the parameters comprise package parameters.

[c6] 6. A method for generating a command file of a group of layout versus schematic (LVS) rules and layout parasitic extraction (LPE) rules to be used by a layout verification tool to verify the layout and the parasitic characteristics of an integrated circuit, the method comprising:
(a) selecting a process from a group of processes;
(b) setting a set of parameters; and
(c) extracting program codes from a plurality of modules according to the selected process and the set of parameters so as to generate a corresponding command file of LVS/LPE rules.

[c7] 7. The method of claim 6 further comprising:
(d) generating a plurality of modules, the plurality of modules comprising:
a header module comprising program codes for settings of a verification tool of different processes;

a layer module comprising program codes for setting layer definitions of different processes;
an operation module comprising program codes of operation definitions of different processes; and
a device module comprising program codes for declaring devices of different processes.

[c8] 8. The method of claim 6 wherein the parameters comprise number of metal layers.

[c9] 9. The method of claim 6 wherein the parameters comprise number of poly-silicon layers.

[c10] 10. The method of claim 6 wherein the parameters comprise package parameters.

[c11] 11. A method for generating a command file of a group of design rule check (DRC) rules or layout versus schematic (LVS) rules and layout parasitic extraction (LPE) rules to be used by a layout verification tool to verify the layout and the parasitic characteristics of an integrated circuit, the method comprising:
(a) choosing whether to generate a command file of DRC rules or a command file of LVS/LPE rules;
(b) selecting a process from a group of processes;
(c) setting a set of parameters; and
(d) extracting program codes from a plurality of modules

according to the choice in step (k), the selected process, and the set of parameters so as to generate a command file of DRC rules or LVS/LPE rules.

[c12] 12. The method of claim 11 further comprising:
(e) generating a plurality of modules, the plurality of modules comprising:
a header module comprising program codes for settings of a verification tool of different processes;
a variable module comprising program codes for setting fabrication parameters of different processes;
a layer module comprising program codes for setting layer definitions of different processes;
an operation module comprising program codes of operation definitions of different processes; and
a device module comprising program codes for declaring devices of different processes;
13. The method of claim 11 wherein the parameters comprise number of metal layers.

[c13] 14. The method of claim 11 wherein the parameters comprise number of poly-silicon layers.

[c14] 15. The method of claim 11 wherein the parameters comprise package parameters.